and a memory **534**, which may be portions of system memory (e.g., DRAM) locally attached to the respective processors. First processor **570** and second processor **580** may be coupled to a chipset **590** via P-P interconnects **552** and **554**, respectively. As shown in FIG. **6**, chipset **590** includes P-P interfaces **594** and **598**.

[0046] Furthermore, chipset **590** includes an interface **592** to couple chipset **590** with a high performance graphics engine **538**, by a P-P interconnect **539**. In turn, chipset **590** may be coupled to a first bus **516** via an interface **596**. As shown in FIG. **6**, various input/output (I/O) devices **514** may be coupled to first bus **516**, along with a bus bridge **518** which couples first bus **516** to a second bus **520**. Various devices may be coupled to second bus **520** including, for example, a keyboard/mouse **522**, communication devices **526** and a data storage unit **528** such as a disk drive or other mass storage device which may include code **530**, in one embodiment. Further, an audio I/O **524** may be coupled to second bus **520**. Embodiments can be incorporated into other types of systems including mobile devices such as a smart cellular telephone, tablet computer, netbook, ultrabook, or so forth.

[0047] FIG. **7** is a block diagram of a system **600** coupled with point-to-point (PtP) system interconnects in accordance with a given cache coherence protocol using QPI links as the system interconnect. In the embodiment shown, each processor **610** is coupled to two PtP links **625** and includes one instance of an integrated memory controller **615** that in turn is coupled to a corresponding local portion of a system memory **620**. Each processor can perform power management techniques using optimized settings obtained from a tuning table in accordance with an embodiment of the present invention. The processors are connected to an input/output hub (IOH) **630** using one link and the remaining link is used to connect the two processors.

[0048] Referring now to FIG. **8**, shown is a block diagram of a system in accordance with another embodiment of the present invention. As shown in FIG. **8**, system **700** may be a partially connected quad processor system in which each processor **710** (each of which may be multicore multi-domain processors) is coupled to each other processor via a PtP link and is coupled to a local portion of memory (e.g., dynamic random access memory (DRAM)) **720** via a memory interconnect coupled to an integrated memory controller **715** of the corresponding processor. In the partially connected system of FIG. **8**, note the presence of two IOHs **730** and **740** such that processors $\mathbf{710}_0$ and $\mathbf{710}_1$ are directly coupled to IOH **730** and similarly processors $\mathbf{710}_2$ and $\mathbf{710}_3$ are directly coupled to IOH **740**.

[0049] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0050] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A processor comprising:

a plurality of cores;

a cache memory;

an interconnect to couple the plurality of cores and the cache memory; and

a power controller to control a plurality of power management features of the processor, wherein the power controller is to receive a workload configuration input regarding a workload, receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon, and update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.

2. The processor of claim **1**, wherein the power controller is to access a power-performance tuning table based on the workload configuration input and the global EPB value, and use information from the power-performance tuning table to update the at least one setting.

3. The processor of claim **2**, wherein the power controller includes a tuning circuit to update the at least one setting of the at least one power management feature responsive to the global EPB value.

4. The processor of claim **3**, wherein the tuning circuit includes a sampler to receive the plurality of EPB values from at least some of the plurality of cores and a combiner to generate the global EPB value from the EPB value from the plurality of cores.

5. The processor of claim **4**, wherein the sampler is to receive the EPB value from a plurality of threads to execute on the at least some of the plurality of cores.

6. The processor of claim **4**, wherein the power controller is to generate a bin value from the global EPB value and to access the power-performance tuning table using the bin value.

7. The processor of claim **3**, wherein the tuning circuit is to update at least one setting of a first power management feature controlled by the power controller, and send a message to an interconnect that couples the processor to a second component of a system to update at least one setting of a second power management feature controlled by the interconnect.

8. The processor of claim **2**, wherein the power-performance tuning table includes a plurality of entries each having a plurality of fields each associated with a range of the EPB value and including a setting for a power management feature.

9. The processor of claim **1**, wherein the processor is to receive at least one EPB value from a baseboard management controller.

10. The processor of claim **1**, wherein the workload configuration input comprises information regarding a workload pattern comprising at least one of a non-uniform